memory objects in the memory." with the following four paragraphs:

--Fig. 3a is schematic illustrating a FIFO operating mode.--

--Fig. 3b is a schematic illustrating a gateway operating mode.--

--Fig. 3c is a schematic illustrating a shared gateway operating mode.--

--Fig. 3d is a schematic illustrating a FIFO gateway operating mode.--

---

In the Claims:

Cancel claim 5.

Claim 1 (amended). In a data transmission system with at least two subscribers, a memory device to be connected, for serial data transfer of binary data objects of a predetermined data width, between the at least two subscribers, comprising:

a multiplicity of memory objects each being identifiable by a respective address;

each said memory object having a data width being at least as large as a predetermined data width of a data object intended for data transfer, an identification region containing the respective address of said memory object, a data region storing the data objects, and a control region containing monitoring and control functions for the data transfer;

at least one FIFO structure containing a plurality of said memory objects and transmitting data in a data-controlled data transfer controlled by the data objects being transmitted.

Claim 22 (amended). A [CAN] Controller Area Network (CAN) bus system, comprising: at least one memory device according to claim 1.

Please Add the Following Claims:

--23. In a data transmission system with at least two subscribers, a memory device to be connected, for serial data transfer of binary data objects of a predetermined data width, between the at least two subscribers, comprising:

a multiplicity of memory objects each being identifiable by a respective address;

each said memory object having a data width being at least as large as a predetermined data width of a data object intended for data transfer and a node selection register indicating a subscriber to which the respective said memory object is assigned;

at least one FIFO structure containing a plurality of said memory objects and transmitting data in a data-controlled data transfer controlled by the data objects being transmitted.--

--24. In a data transmission system with at least two subscribers, a memory device to be connected, for serial data transfer of binary data objects of a predetermined data width, between the at least two subscribers, comprising:

a multiplicity of memory objects each being identifiable by a respective address;

each said memory object having a data width being at least as large as a predetermined data width of a data object intended

for data transfer and a gateway control register defining an operating mode of the respective said memory object;

at least one FIFO structure containing a plurality of said memory objects and transmitting data in a data-controlled data transfer controlled by the data objects being transmitted.--

--25. In a data transmission system with at least two subscribers, a memory device to be connected, for serial data transfer of binary data objects of a predetermined data width, between the at least two subscribers, comprising:

a multiplicity of memory objects each being identifiable by a respective address and a node selection register indicating a subscriber to which the respective said memory object is assigned, and a gateway control register defining an operating mode of the respective said memory object, and wherein a content of said gateway control register and a content of said node selection register are configurable via at least one of the subscribers and a central processing unit;

each said memory object having a data width being at least as large as a predetermined data width of a data object intended for data transfer;